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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/810,208	WONG ET AL.	
	Examiner	Art Unit	
	Chandrahas Patel	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30 and 32-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30 and 32-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/11/2009, 4/9/2009, 5/19/2009, 7/30/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Regarding to Arguments

1. Applicant's arguments see pages 13-19, filed 6/15/2009, with respect to claims 20-30, 32-44 and 47 have been fully considered and are persuasive. The rejection of 2/13/2009 has been withdrawn.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-15, 18, 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maher, III et al. (USPN 6,654,373) in view of Scholten (USPN 7,126,956).

Regarding claim 1, Maher, III teaches a circuit for aggregating a plurality of input data streams from first processors into one data stream for a second processor, **[Fig. 2, 100]**, the circuit comprising: a plurality of ingress data ports, each ingress data port adapted to receive an input data stream, each input data stream formed of ingress data packets **[Fig. 2, 102, Col. 6, lines 5-14, lines 10-14]**, each ingress data packet including priority factors coded therein **[Col. 6, lines 22-25, type or protocol can be a priority factor as discussed in applicant's specification]**; an aggregation module coupled to the plurality of ingress data ports, the aggregation module adapted to analyze and combine the plurality of input data steams into one aggregated data stream in response to the priority factors **[Fig. 2, 140, Col. 6, lines 15-25]** and to generate a packet descriptor comprising a reference to a memory location of its analyzed data packet **[Col. 9, lines 37-54, the context is the memory location of the data packet]**;

a memory coupled to the aggregation module, the memory adapted to store analyzed data packets **[Fig. 2, 112]**; the memory comprising a plurality of priority queues each provided for a corresponding priority class, adapted to store the packet descriptor of each of the analyzed data packets classified to the corresponding priority class, the packet descriptor containing a reference to the memory location of its analyzed data packet in the memory **[Fig. 2, 116, Col. 7, lines 34-53, packets are stored in different queues according to their priority and Col. 9, lines 37-54 teaches that the context is the memory location of the data packet]**; and an output data port coupled to the aggregation module, the output data port adapted to output the aggregated data stream to the second processor **[Fig. 2, 120]**.

However, Maher, III does not teach each data port is coupled to a corresponding processor and receives data from its corresponding processor, and an aggregation module receives the plurality of input data streams from the first processors using the plurality of ingress data ports, wherein an input data stream from a first processor is received via the ingress data port coupled to the first processor.

Scholten teaches each data port is coupled to a corresponding processor and receives data from its corresponding processor, and an aggregation module receives the input data streams from the first processors using the plurality of ingress data ports, wherein an input data stream from a first processor is received via the ingress data port coupled to the first processor **[Col. 7, lines 47-49, plurality of transmit FIFOs receive the data stream from plurality of processors coupled to them as can be seen in Fig. 3, 310 transmit FIFOs are coupled to ingress data processors 314]**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to couple a processor to each data port so that each processor can format data for its corresponding port **[Col. 7, lines 49-53]**.

Regarding claim 2, Maher, III teaches each of the first processors and the second processor transmits and receives a data stream through a logical interface providing logical interconnection between a Media Access Control sub layer (MAC) and a Physical layer (PHY) **[Fig. 2, 102, 120, Abstract]**.

Regarding claim 3, Scholten teaches the first processors are Layer-2 switching processors **[Col. 7, lines 53-57]**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a Layer-2 switching processor since data received from physical layer has to be converted into layer 2 data.

Regarding claim 4, Maher, III teaches the second processor is a data packet processor **[Fig. 4, 418]**.

Regarding claim 5, Maher, III teaches memory is an external buffer memory **[Fig. 2, 112]**.

Regarding claims 6, 14, Maher, III teaches an egress data input port adapted to receive a data stream from the second processor, the data stream formed of egress data packets **[Fig. 4, 414 outputs the data to 404 through single port]**; a plurality of egress data output ports, each adapted to output an output data stream to a corresponding one of the first processors **[Fig. 4, multiple outputs shown going out of 404 to 402]**; and a forwarding module coupled between the egress data input port

and the egress data output port, the forwarding module adapted to forward an egress data packet in the data stream from the second processor to one of the egress data output port in response to destination information associated with the egress data packet **[Fig. 4, 404, Col. 11, lines 14-17]**.

Regarding claim 7, Maher, III teaches ingress data ports include a first data port for receiving a first input data stream and a second data port for receiving a second input data stream **[Fig. 2, 102, Col. 6, lines 5-10]**; and aggregation module includes: a first packet analyzer coupled to the first data port, adapted to classify each of the ingress data packets in the first data stream into one of predetermined priority classes based on the priority factors **[Fig. 2, 110, Col. 7, lines 41-44]**; a second packet analyzer coupled to the second data port, adapted to classify each of the ingress data packets in the second data stream into one of predetermined priority classes based on the priority factors **[Fig. 2, 110, Col. 7, lines 41-44]**; a queue module having a selection logic implementing a queue scheme, adapted to arbitrate and select a packet descriptor from among the priority queues **[Fig. 2, 116, packets are stored in 132, Col. 7, lines 34-44]**; a first write interface coupled to first packet analyzer, adapted to write the analyzed data packets into the memory at the memory location indicated by the corresponding packet descriptor **[Col. 7, lines 34-36]**; a second write interface coupled to second packet analyzer, adapted to write the analyzed data packets into memory at the memory location indicated by the corresponding packet descriptor **[Col. 7, lines 34-36]**; a common read interface coupled to queue selection logic, adapted to read a data packet corresponding to the selected packet descriptor from memory **[Col. 8, lines 7-**

14]; and an output module to send the data packets read from memory to output data port as the aggregated data stream **[Fig. 2, 120]**.

Regarding claim 8, Maher, III teaches packet analyzer includes a data decoder coupled to ingress data port to decode a header of each ingress data packet to extract the priority factors **[Fig. 2, 104, Col. 6, lines 15-25]**.

Regarding claim 9, Maher, III teaches a read buffer is coupled to common read interface **[Fig. 2, 136]**.

Regarding claim 10, Maher, III teaches a data encoder is coupled to read buffer that encodes the data packets into an interface format corresponding to the first interface before sending from the output port **[Col. 8, lines 26-28]**.

Regarding claim 11, Maher, III teaches a write buffer coupled between first packet analyzer and first write interface **[Fig. 2, 118]**.

Regarding claims 12, 13, 15, Scholten teaches a flow control module is adapted to assert a flow control if an amount of data stored in buffer exceeds a threshold **[Col. 8, lines 7-29]**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to assert a flow control signal if buffer exceeds a threshold so that port is not blocked if overflow occurs at a particular channel **[Col 8, lines 7-29]**.

Regarding claim 18, Maher, III teaches the priority factors include an indication of whether the ingress packet contains protocol data or not **[Fig. 2, 140, Col. 6, lines 15-25]**.

Regarding claim 46, Maher, III teaches a method for aggregating a plurality of input data streams **[Fig. 2, 100]**, the method comprising: receiving an input data stream, each input data stream formed of ingress data packets **[Fig. 2, 102, Col. 6, lines 5-14]**, each ingress data packet including priority factors coded therein **[Col. 6, lines 22-25, type or protocol can be a priority factor as discussed in applicant's specification]**; generating an aggregated data stream by combining the plurality of input data steams into one aggregated data stream in response to the priority factors, the priority factors including an indication of whether the ingress packet contains protocol data or not **[Fig. 2, 140, Col. 6, lines 15-25]**, classifying each of the ingress data packets into one of a plurality of priority classes based on the priority factors included in the ingress data packet **[Col. 7, lines 34-53, packets are stored in different queues according to their priority]**; and outputting the aggregated data stream **[Fig. 2, 120]**.

However, Maher, III does not teach providing, for each first processor, an analyzer corresponding to the first processor, the analyzer being separate from the first processor and located in a communication path between the first processor and the second processor; wherein the generating comprises, for each first processor, receiving the input data stream from the first processor at an analyzer corresponding to the first processor, and analyzing the input data stream received from the first processor using the analyzer.

Scholten teaches providing, for each first processor, an analyzer corresponding to the first processor, the analyzer being separate from the first processor and located in a communication path between the first processor and the second processor **[Col. 8,**

lines 7-37, analyzer is provided for each processor for determining FIFO fill level and for determining whether data can be transmitted on that port or not]; wherein the generating comprises, for each first processor, receiving the input data stream from the first processor at an analyzer corresponding to the first processor, and analyzing the input data stream received from the first processor using the analyzer **[Col. 8, lines 7-37, receives data and analyzes for buffer fullness for transmission purposes]**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have analyzer so that data can be analyzed for transmission purposes and buffer fill level information **[Col 8, lines 7-37]**.

4. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maher, III et al. (USPN 6,654,373) in view of Scholten (USPN 7,126,956) as applied to claim 15 above, and further in view of Manaka et al. (USPN 6,421,352).

Regarding claim 16, the references teach a circuit as discussed in rejection of claim 15.

However, the references do not teach inserting a pause control packet when queue exceeds a threshold.

Manaka teaches inserting a pause control packet when queue exceeds a threshold **[Col. 2, lines 25-28]**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to insert a pause control packet when congestion occurs so that only one of the LAN connections is interrupted instead of all **[Col. 4, lines 62-66]**.

5. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maher, III et al. (USPN 6,654,373) in view of Scholten (USPN 7,126,956) and Abbas et al. (USPN 6,810,046).

Regarding claim 17, the references teach a circuit as discussed in rejection of claim 1.

However, the references do not teach the aggregation module is implemented by a programmable device.

Abbas teaches the aggregation module is implemented by a programmable device **[Fig. 3, 540]**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a FPLD implement the device so that configuration of the aggregation module can be changed after it has been fabricated and can be programmed to match the need of system **[Col. 7, lines 49-53]**.

6. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maher, III et al. (USPN 6,654,373) in view of Scholten (USPN 7,126,956) as applied to claims 18, 44 and 62 above, and further in view of Mackiewich et al. (USPN 7,212,536).

Regarding claim 19, Maher, III teaches priority factors include per-port priority **[Col 3, lines 34-37]**.

However, Maher, III does not teach priority factors include VLAN priority.

Mackiewich teaches priority factors include VLAN priority **[Abstract]**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have VLAN priority so that different treatment can be given to connections with different priority **[Col. 1, lines 7-11]**.

Regarding claim 45, Maher, III teaches priority factors comprise protocol filter priority **[Col. 1, lines 6-8]**, per-port priority **[Col 3, lines 34-37]**.

However, Maher, III does not teach priority factors include VLAN priority.

Mackiewich teaches priority factors include VLAN priority **[Abstract]**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have VLAN priority so that different treatment can be given to connections with different priority **[Col. 1, lines 7-11]**.

7. Claims 20-30, 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maher, III et al. (USPN 6,654,373) in view of Scholten (USPN 7,126,956) and Rajkumar et al. (USPN 7,391,769).

Regarding claim 20, Maher, III teaches a circuit for aggregating a plurality of input data streams **[Fig. 2, 100]**, the circuit comprising: a first data link adapted to receive the input data stream via a first data link having a first bandwidth, the input data stream formed of ingress data packets **[Fig. 2, 102, Col. 6, lines 5-14]**, each ingress data packet including priority factors coded therein **[Col. 6, lines 22-25, type or protocol can be a priority factor as discussed in applicant's specification]**; the aggregation module adapted to analyze and selectively recombine the ingress data packets in response to the priority factors so as to generate an aggregated data **[Col. 7,**

lines 41-52]; a memory coupled to the aggregation module, the memory adapted to store analyzed data packets **[Fig. 2, 112]**; and a second data link coupled to the aggregation module, the second data link adapted to output the aggregated data stream from the aggregation module **[Fig. 2, 120, 126]**.

However, Maher, III does not teach generating an aggregated data stream for a second data link having a second bandwidth smaller than the first bandwidth; a first data link is coupled to first processor and a second data link is coupled to second processor; the first data link is adapted to receive the input data stream from the first processor via the first data link; and a second data link outputting the data stream to the second processor.

Scholten teaches a first data link is coupled to first processor and a second data link is coupled to second processor **[Fig. 3, 314, 316]**; the first data link is adapted to receive the input data stream from the first processor via the first data link **[Col. 7, lines 47-49, as can be seen in Fig. 3, 310 transmit FIFOs are coupled to ingress data processors 314 to receive data from 314]**; and a second data link outputting the data stream to the second processor **[Fig. 3, 312 outputs data to plurality of egress processors 316]**. Rajkumar teaches a second data link coupled to the aggregation module, second data link having a second bandwidth smaller than the first bandwidth **[Fig. 1A, output is couple to aggregator 104, Col. 4, lines 50-53, output rate is lower than input rate]**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to generate a data stream having less bandwidth than first

bandwidth since only portion of the data that is required is aggregated so information that is being output is less than the information coming in thus bringing down the output data rate **[Fig. 2, 202]** and have processors on input and output port so that each processor can format data for transmission and reception **[Col. 8, lines 38-50]**.

Regarding claim 21, Maher, III teaches each of the first processors and the second processor transmits and receives a data stream through a logical interface providing logical interconnection between a Media Access Control sub layer (MAC) and a Physical layer (PHY) **[Fig. 2, 102, 120, Abstract]**.

Regarding claim 22, Maher, III teaches memory is an external buffer memory **[Fig. 2, 112]**.

Regarding claim 23, Maher, III teaches aggregation module comprising: a packet analyzer adapted to classify each of the ingress data packets into one of predetermined priority classes based on the priority factors **[Fig. 2, 110, Col. 7, lines 41-44]**; a queue module comprising a plurality of priority queues each provided for the corresponding priority class, adapted to store a packet descriptor of each of the analyzed data packets classified to the corresponding priority class, the packet descriptor containing a reference to a memory location of its analyzed data packet in the memory, and a selection logic implementing a queue scheme, adapted to arbitrate and select a packet descriptor from among the priority queues **[Fig. 2, 116, packets are stored in 132, Col. 7, lines 34-44]**; a read interface coupled to the queue module, adapted to read a data packet corresponding to the selected packet descriptor from the

memory **[Col. 8, lines 7-14]**; and an output module to send the data packets read from the memory to the second data link as the aggregated data stream **[Fig. 2, 120]**.

Regarding claim 24, Maher, III teaches packet analyzer includes a data decoder coupled to ingress data port to decode a header of each ingress data packet to extract the priority factors **[Fig. 2, 104, Col. 6, lines 15-25]**.

Regarding claim 25, Maher, III teaches a read buffer is coupled to common read interface **[Fig. 2, 136]**.

Regarding claim 26, Maher, III teaches a data encoder is coupled to read buffer that encodes the data packets into an interface format corresponding to the first interface before sending from the output port **[Col. 8, lines 26-28]**.

Regarding claim 27, Maher, III teaches a write interface coupled to the packet analyzer, adapted to write the analyzed data packets into the memory at the memory location indicated by the corresponding packet descriptor **[Col. 7, lines 34-46]**.

Regarding claim 28, Maher, III teaches a write buffer coupled between first packet analyzer and first write interface **[Fig. 2, 118]**.

Regarding claim 29, 30, Scholten teaches a flow control module is adapted to assert a flow control if an amount of data stored in buffer exceeds a threshold **[Col. 8, lines 7-29]**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to assert a flow control signal if buffer exceeds a threshold so that port is not blocked if overflow occurs at a particular channel **[Col 8, lines 7-29]**.

Regarding claim 47, Maher, III teaches a method for aggregating data packets **[Fig. 2, 100]**, the method comprising: receiving an input data stream from the first port via a first data link having a first bandwidth, the input data stream formed of ingress data packets **[Fig. 2, 102, Col. 6, lines 5-14]**, each ingress data packet including priority factors coded therein **[Col. 6, lines 22-25, type or protocol can be a priority factor as discussed in applicant's specification]**; generating an aggregated data stream by analyzing and selectively recombining the ingress data packets in response to the priority factors, the priority factors including an indication of whether the ingress packet contains protocol data or not **[Fig. 2, 140, Col. 6, lines 15-25]**; and outputting the aggregated data stream to a second port via a second data link having a second bandwidth **[Col. 7, lines 47-52]**.

However, Maher, III does not teach generating an aggregated data stream for a second data link having a first bandwidth greater than the second bandwidth and first data port is coupled to first processor and second data port is coupled to second processor.

Scholten teaches first data port is coupled to first processor and second data port is coupled to second processor **[Fig. 3, 314, 316]**. Rajkumar teaches a second data link coupled to the aggregation module, first data link having a first bandwidth greater than the second bandwidth **[Fig. 1A, output is couple to aggregator 104, Col. 4, lines 50-53, output rate is lower than input rate]**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to generate a data stream having less bandwidth than first

bandwidth so that users only utilize the bandwidth needed at a particular time **[Col. 1, lines 53-57]** and have processors on first and second port so that each processor can format data for transmission and reception **[Col. 8, lines 38-50]**.

8. Claims 32-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maher, III et al. (USPN 6,654,373) in view of Scholten (USPN 7,126,956) and Walsh (USPN 7,561,590).

Regarding claim 32, Maher, III, teaches a method for aggregating a plurality of input data streams **[Fig. 2, 100]**, the method comprising: receiving an input data stream from, each input data stream formed of ingress data packets **[Fig. 2, 102, Col. 6, lines 5-14]**, each ingress data packet including priority factors coded therein **[Col. 6, lines 22-25, type or protocol can be a priority factor as discussed in applicant's specification]**; analyzing and classifying each of the ingress data packets into one of predetermined priority classes based on the priority factors **[Fig. 2, 140, Col. 6, lines 15-25]**; storing an analyzed data packet in a memory **[Fig. 2, 112]**; generating a packet descriptor for the analyzed ingress data packet, the packet descriptor containing a reference to a memory location of its analyzed data packet stored in the memory **[Col. 9, lines 32-36, context is memory location for packets]**; arbitrating and selecting a packet from among the priority queues using selection logic implementing a queue scheme **[Col. 9, lines 47-51]**; reading a data packet corresponding to the selected packet from the memory **[Col. 9, lines 47-51]**; and sending the data packets read from the memory as an aggregated data stream **[Col. 8, lines 7-14]**.

However, Maher III does not teach first processor and second processors are used for sending and receiving data streams; and placing the packet descriptor in a priority queue corresponding to the priority class of the data packet.

Scholten teaches first processor and second processors are used for sending and receiving data streams **[Fig. 3, 314, 316]**. Walsh teaches placing the packet descriptor in a priority queue corresponding to the priority class of the data packet **[Col. 4, lines 28-41, pointers for frames corresponding to that frame are stored in the priority queue]**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have processors for input and output so that each processor can format data for transmission and reception **[Col. 8, lines 38-50]** and to store pointers corresponding to the frames so that the switching operations can be done by controlling pointers pointing to memory **[Col. 2, lines 35-36]**.

Regarding claim 33, Maher, III teaches packet analyzer includes a data decoder coupled to ingress data port to decode a header of each ingress data packet to extract the priority factors **[Fig. 2, 104, Col. 6, lines 15-25]**.

Regarding claim 34, Maher, III teaches buffering the analyzed data packet in a write buffer before storing in the memory **[Fig. 2, 118]**.

Regarding claims 35, 38, Scholten teaches a flow control module is adapted to assert a flow control if an amount of data stored in buffer exceeds a threshold **[Col. 8, lines 7-29]**.

Regarding claim 36, Maher, III teaches buffering the data packet read from the memory in a read buffer **[Fig. 2, 118]**.

Regarding claim 37, Maher, III teaches a data encoder is coupled to read buffer that encodes the data packets into an interface format corresponding to the first interface before sending from the output port **[Col. 8, lines 26-28]**.

Regarding claim 39, Maher, III teaches memory is an external buffer memory **[Fig. 2, 112]**.

Regarding claim 40, Maher, III teaches each of the first processors and the second processor transmits and receives a data stream through a logical interface providing logical interconnection between a Media Access Control sub layer (MAC) and a Physical layer (PHY) **[Fig. 2, 102, 120, Abstract]**.

Regarding claim 41, Maher, III teaches analyzing and classifying, generating, and storing are performed separately for each data stream **[Col. 7, lines 38-40, Fig. 2, 110]**.

Regarding claim 42, Maher, III teaches packet descriptors from each stream of a same priority class are placed in the same priority queue for that priority class **[Col. 7, lines 41-53]**.

Regarding claim 43, Maher, III teaches arbitrating and selecting, reading, and sending is performed as a single data channel **[Fig. 2, Path 126]**.

Regarding claim 44, Maher, III teaches protocol filtering to determine if the ingress data packet is a certain protocol packet **[Col. 6, lines 22-25]**.

9. Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maher, III et al. (USPN 6,654,373) in view of Scholten (USPN 7,126,956) and Walsh (USPN 7,561,590) as applied to claim 44 above, and further in view of Mackiewich et al. (USPN 7,212,536).

Regarding claim 45, Maher, III teaches priority factors comprise protocol filter priority **[Col. 1, lines 6-8]**, per-port priority **[Col 3, lines 34-37]**.

However, Maher, III does not teach priority factors include VLAN priority.

Mackiewich teaches priority factors include VLAN priority **[Abstract]**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have VLAN priority so that different treatment can be given to connections with different priority **[Col. 1, lines 7-11]**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chandrahas Patel whose telephone number is (571)270-1211. The examiner can normally be reached on Monday through Thursday 7:30 to 17:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ricky Ngo/
Supervisory Patent Examiner, Art Unit 2416

/Chandrahas Patel/
Examiner, Art Unit 2416